reading the instruction or data in accordance with the address for the instruction or the address for the data with the first unit when the pseudo instruction is detected;

storing the instruction or the data in a buffer; and

executing the stored instruction with a second unit.

3. (Twice Amended) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel to the memory, and the method further comprising a step of storing the instruction and data read from the memory in the first buffer and storing the instruction or data included in the detected pseudo instruction in the second buffer.

8. (Thrice Amended) A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program read from the memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data;

a first unit including,

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program read from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for reading the instruction or data in accordance with the

address for the instruction or the address for the data when the pseudo instruction is detected and storing the instruction or the data in the buffer; and

a second unit connected to the buffer, for executing the instruction stored in the buffer.

9. (Twice Amended) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel to the memory, wherein the first buffer stores the instruction and data read from the memory, and the second buffer stores the instruction or data included in the detected pseudo instruction.

14. (Thrice Amended) A device for detecting a pseudo instruction present before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, and wherein the device is independent of an instruction execution unit for executing the specific instruction, the device comprising:

a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode when the pseudo instruction is detected and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the

detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

24. (Amended) The method of claim 1, wherein the at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

25. (Amended) The method of claim 1, further comprising executing a no-operation (NOP) instruction when the pseudo instruction is detected.

26. (Amended) The method of claim 1, further comprising the second unit ignoring an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data to skip the pseudo instruction.

27. (Amended) The microcontroller of claim 8, wherein the at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

28. (Amended) The microncontroller of claim 8, wherein the second unit executes a no-operation (NOP) instruction when the pseudo instruction is detected.

29. (Amended) The microcontroller of claim 8, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data to skip the pseudo instruction.

30. (Amended) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

prefetching the instruction or data in accordance with the detection of the pseudo instruction with the first unit when the pseudo instruction is detected; and

executing a no-operation (NOP) instruction when the pseudo instruction is detected with a second unit.

31. (Amended) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit when the pseudo instruction is detected;

prefetching the instruction or data in accordance with the detection of the pseudo instruction with the first unit; and

when receiving the address for the at least one instruction or the address for data a second unit, which is independent of the first unit, skipping the pseudo instruction and executing the prefetched instruction.

32. (Amended) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data when the pseudo instruction is detected; and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction.

33. (Amended) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one

instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data when the pseudo instruction is detected; and

a second unit for executing the prefetched instruction, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data to skip the pseudo instruction.

34. (Amended) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit reads the instruction or data in accordance with the address for the instruction or the address for the data when the pseudo instruction is detected, wherein the first unit includes a buffer for storing the instruction or the data; and

a second unit for executing the stored instruction.